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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/328,800	06/09/1999	HIROSHI ITO	H-782	7315

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/328,800	ITO ET AL.	
	Examin r	Art Unit	
	Fred Ferris	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-9,13-16 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5, 6, 8, 9, 13, 14, 16, 20-22* is/are rejected.

7)☐ Claim(s) *7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 13 November 2003 (paper #12) has been entered. Claims 1, 5-9, 13-16, and 20-22 are currently pending in this application. The applicants have canceled claims 2-4, 10-12, 17-19 and 23.

Response to Arguments

2. Applicants arguments filed on 13 November 2003 (paper #12) have been fully considered but are now considered moot based on the new grounds for rejection.

Regarding applicant's response to 102(b) rejection: The examiner withdraws the previous 102(b) rejection in view of applicant's amendment to the claims. However, new 102(b) rejections have now been applied. (please see new 102(b) rejections below)

Regarding applicant's response the 103(a) rejections: The examiner withdraws the previous 103(a) rejection in view of applicant's amendment to the claims. However, the examiner has now applied new 103(a) rejections based on new prior art. (please see new 103(a) rejections below)

Claim Int rpretation

3. The claimed invention is disclosed to be a logic module used for logic emulation and verification of electronic circuits. The device falls into the broad category known in the art as circuit emulators and in-circuit emulators (ICE). The logic module (a circuit board) contains numerous programmable large scale integrated circuits (LSI's), programmable cross-point-switches (allowing programmable connections between LSI's), and connectors for external connection and connection to an enhanced logic emulation board. A structure using popular industry techniques for multiple module staging (stacking/platform) and cooling of IC's in the structure is also described.

The examiner notes that, in general, the independent claim limitations are drawn to well known and commonly used techniques used in the art, and in the cited prior art, for the design of emulation printed circuit modules. These include:

- *Connectors for external connections*
- *Programmable LSI's (programmed logic)*
- *Switching LSI's (cross point switch)*
- *Board wiring*
- *Terminal lands for LSI's*
- *Printed circuit thru-holes*
- *Circuit card stacking*
- *Radiation plates, heat sinks, metal spacers*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 6, 8, 9, 13, 14, 16, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent issued to Ikeda et al in view of U.S. Patent 5,572,710 issued to Asano et al in further view U.S. Patent 6,016,563 issued to Fleisher.

The factual inquiries set forth in Graham ***v.*** *John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:*

1. *Determining the scope and contents of the prior art.*
2. *Ascertaining the differences between the prior art and the claims at issue.*
3. *Resolving the level of ordinary skill in the pertinent art.*
4. *Considering objective evidence present in the application indicating obviousness or nonobviousness.*

Independent claims are drawn to a ***logic emulation module*** *comprising:*

- ***programmable LSI's*** *capable of* ***programming logic***
- ***switching LSI's*** *(elements) capable of* ***programming connections***
- ***connectors*** *for* ***external electrical connection***
- *a* ***board*** *(with* ***wiring****) on which to* ***mount programmable LSI's***
- *lines from* ***connectors to programmable LSI's*** *and* ***linking programmable LSI's by way of switching LSI's***
- ***LSI*** *logically* ***equivalent functions*** *on module for* ***logic verification***
- *programmable LSI's connected to other programmable LSI's via switching LSI's*
- *Stacking type connectors*
- *terminal lands, and multiple (1st, 2nd, 3rd, 4th, etc.) wiring schemes*

Per independent claims 1, 13, 16, and 20: Ikeda discloses a ***programmable logic emulation system*** *(module) constructed of a* ***circuit board*** *(with board wiring) having* ***through holes*** *and* ***programmable logic devices*** *(LSI's) connected via field* ***programmabl logic arrays (FPLA), int rconn ct*** *(cross-point-****switch s,****) containing* ***conn ctors*** *for* ***ext rnal c nn ction*** *used for* ***logic emulation*** *of* ***equivalent***

functions *and* ***v rification****. (Abstract, Summary of Invention, CL2-L49-65, CL3-L1-41, CL8-L11-CL10-L35, Figs. 6-8)*

Ikeda does not explicitly teach lines from connectors to programmable LSI's and linking programmable LSI's by way of switching LSI's.

Asano also discloses a programmable logic emulation system having programmable logic devices (LSI's) connected via field programmable logic arrays (FPLA), interconnect (cross-point-switches), and containing connectors for external connection used for logic emulation of equivalent functions and verification. However, Asano further discloses a system with lines from ***external connectors*** *directly to* ***programmable LSI's*** *and the ability to* ***link the programmable LSI's*** *by way of* ***switching LSI's*** *(cross point switch) to* ***other programmable LSI's*** *using multiple (1st, 2nd, 3rd, 4th, etc.) wiring schemes. (Abstract, Summary of Invention, CL3-L25-65, CL6-L55-65, CL8-L12-53, CL20-L12-55, Figs.3, 7, 14, 22, 26, 27, 30-32, 41)*

Ikeda further does not explicitly teach the use of stacking type connectors on emulation modules.

Fleisher also discloses a programmable logic emulation system having programmable logic devices (LSI's) connected via field programmable logic arrays (FPLA), interconnect (cross-point-switches), and containing connectors for external connection used for logic emulation of equivalent functions and verification. However, Fleisher further teaches the use of ***stacking type connectors*** *on emulation modules. (Abstract, Summary of Invention, CL2-L35-65, CL3-L45-51, CL5-L25-CL6-L35, Figs. 3-7 especially figures 3 and 5)*

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Ikeda relating to a programmable logic emulation system having programmable logic devices (LSI's) connected via field programmable logic arrays (FPLA), interconnect (cross-point-switches), and containing connectors for external connection used for logic emulation of equivalent functions and verification, with the teachings of Asano relating to an emulation system with lines from external connectors directly to programmable LSI's and the ability to link the programmable LSI's by way of switching LSI's (cross point switch) to other programmable LSI's using multiple (1st, 2nd, 3rd, 4th, etc.) wiring schemes, and to further modify the teachings on Ikeda with the teachings of Fleisher relating to use of stacking type connectors on emulation modules, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many emulation systems available in the market place and large amounts of money being spent in product development and improvement. (see Fleisher column 1, line 45, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Ikeda with the teachings of Asano, and to further modify the teachings of Ikeda with the teachings of Fleisher, in order to reduce development time and cost.

Regarding dependent claims 5, 6, 8, 9, 14, and 21: This group of claims includes limitations relating to, LSI's mounting, thru-holes, stack connectors (side), and control signals which are rejected using the same reasoning as previously cited above.

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable in further view of U.S. Patent 6,005,771 issued to Bjorndahl et al.

Regarding independent claim 22: Bjorndahl discloses a multi chip module with integrated circuits and radiation plates on both sides of the module covering the integrated circuits. (Abstract, Summary of Invention, CL2-L31-65, Figs, 1 and 2) It would have been obvious (as cited above) to cover the emulation module with radiation plates (i.e. shielding) secured at four corners using metal spacers and a flexible heat conduction sheet as a design choice in order to provide proper cooling and EMI shielding for the LSI's.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 13 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 5,604,888 issued to Kiani-Shabestari et al.

Regarding independent claim 13: Kiani-Shabestari discloses a programmable logic emulation system having programmable logic devices (LSI's) connected via programmable logic arrays (PLA), interconnect (cross-point-switches), and connectable to other LSI's containing terminal lands and connectors for external connection used for logic emulation of equivalent functions and verification. (Abstract, Summary of Invention, CL3-L21-65, CL4-L15-27, 53-65, Figs. 1, 3)

7. Claim 16 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,016,563 issued to Fleisher.

Regarding independent claim 16: Fleisher discloses a programmable logic emulation system having programmable logic devices (LSI's) connected via field programmable logic arrays (FPLA), interconnect (cross-point-switches), and containing connectors for external connection used for logic emulation of equivalent functions and verification. Fleisher further teaches the use of stacking type connectors on emulation modules. (Abstract, Summary of Invention, CL2-L35-65, CL3-L45-51, CL5-L25-CL6-L35, Figs. 3-7 especially figures 3 and 5)

Allowable Subject Matter

8. Claims 7, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The examiner has noted that, in general, the independent claim limitations are drawn to well known and commonly used techniques used in the art, and in the cited prior art, for the design of emulation printed circuit modules. These include:

- *Connectors for external connections*
- *Programmable LSI's (programmed logic)*
- *Switching LSI's (cross point switch)*
- *Board wiring*
- *Terminal lands for LSI's*
- *Printed circuit thru-holes*
- *Circuit card stacking*
- *Radiation plates, heat sinks, metal spacers*

Accordingly, are encouraged to amend independent claim 1 to include the limitations of objected to claim 7 (and intervening claims), and to amend independent claim 13 to include the limitations of dependent claims 14 and 15. At such time, the examiner would favorably consider the allowance claims 1, 5-9, and 13-15.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,006,022 issued to Rhim et al teaches in-circuit emulation and verification.

U.S. Patent 5,331,571 issued to Aronoff et al teaches emulation of integrated circuits.

U.S. Patent 5,339,262 issued to Rostoker et al teaches in-circuit testing and verification.

U.S. Patent 5,462,442 issued to Umemura et al teaches stacked printed circuit boards.

U.S. Patent 5,575,686 issued to Noschese teaches stacked printed circuit boards.

U.S. Patent 5,574,338 issued to Babier et al teaches programmable interconnection.

U.S. Patent 5,748,875 issued to Tzori teaches logic simulation and emulation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

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